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| **O:\1 - PROPOSALS & PUBLICATIONS\PROPOSAL_DEPT\Intellisense\Intellisense Logo\IS-logo - fin.png** | | | **ELECTRO-OPTICS SYSTEMS (DEPT. 28)**  **REPORT ROUTING SLIP** | | | | | |
| **Job No.:** | 33059 | | | **Author:** | Alex Genusov | **Due Date:** | 07/15/19 | |
| **Nickname:** | ARMY PAN-UAS II | | | **PI:** | Alex Genusov |  |  | |
| **Type of Report:** SBIR Strategic  Phase I Phase II | | | | | Monthly Report #1 | | | |
|  | | Action/Comments | | | | Approval | | Date & Time |
| **P&P TEAM:**  **Check In / BP** | |  | | | Start No. of pages: 13  Format specific to contract requirements  Requested financial info 7/8 | Jenny Greer | | 07/11/19 @ 9:45am |
| **Editor:**  To:  Date/Time: | | Future plans need to be updated | | | Task progress matches schedule.  Previous report reviewed for task progress/issues.  Future plans correlate with tasks/milestones. | Heather Stanfield | | 7/11/2019 10:47 AM |
| **Director:**  To:  Date/Time: | |  | | | This report contains original work. It doesn’t repeat or duplicate results of previously reported work unless necessary for explanatory purposes or clarity. |  | |  |
| **Author:**  To:  Date/Time: | | Addressed the comments. Figures 2-4 and 2-5 are from consultant and we might not have time to replace them.  Financial section is to be updated. | | | This report contains original work. It doesn’t repeat or duplicate results of previously reported work unless necessary for explanatory purposes or clarity. | Alex Genusov | | 7/12/2019 3:21 PM |
| **Dan edmans:**  **Date/Time:** | | Figure 2-4 is poor quality (unprofessional) and needs to be replaced.  Use the symbols for the electrical parameters epsilon and delta for permittivity and loss tangent:   and tan | | | | Daniel Edmans | | 7/12/19 |
| **VP/GM:**  Date/Time: | | To author, please address my comment. I don’t need to see the report again. | | | This report contains original work. It doesn’t repeat or duplicate results of previously reported work unless necessary for explanatory purposes or clarity.  Addressed any remaining issues.  Checked graphics. | Min-Yi Shih | | 07/12/2019 @ 11:10 am |
| **P&P Manager:**  Date/Time: | | Inserted financials | | | Format specific to contract requirements  Cover Sheet contract info verified.  Tasks reviewed against performance sched.  All refs & callouts verified. | RiAnne  Ostrander | | 07/15 @ 12pm |
| **P&P TEAM:**  **Finalize** | | n/a | | | End No. of pages:  Updated financials inserted  Checked callouts/references |  | |  |
| **Submitted for Distribution: (Upload, email, mail / Color copies / CD(s))** | | | | | |  | |  |
| **Notes/Special Instructions:**  *Contract contains a 4 month transition phase (like a Phase I Option; 02/01/19 – 05/31/19) and 24 months for Phase II (06/01/19 – 05/31/21).*  *CLIN 0002: The Phase I Transition Phase requires 3 monthly reports + 1 draft final report + 1 final report.*  *Monthly Reports: DI-MGMT-80227; contractor format*  *Final Reports: ANSI DI-MISC-090711A; contractor format*  *Distribution Statement D: Distribution authorized to the Department of Defense and DoD contractors only. Reason: To protect technical/operational data or information. Other requests shall be referred to RDER-NVG-MS.*  *Contract requires a sexual harassment plan (due 6/15/19) – 3/8/19 Angie is checking with HR to see if they can write/provide it.* | | | | | | | | |

**Portable Anti-UAS Device (PAN-UAS)**

*SBIR Phase II Monthly Report #1 – July 15, 2019*

CDRL B001

Period of Performance: February 1, 2019 – May 31, 2021

Report Period: June 1, 2019 – June 30, 2019

SBIR Topic Number: A17-098

Contract Number: W909MY-19-C-0006

**Technical Monitor:**

U.S. Army RDECOM, CERDEC

Night Vision and Electronic Sensors Directorate (NVESD)

RDER-NVG-MS

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**Principal Investigator:**

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| **SBIR DATA RIGHTS**  Contract No.: W909MY-19-C-0006  Contractor Name: Intellisense Systems, Inc.  Contractor Address: 20600 Gramercy Place, Torrance, CA 90501-1821  Expiration of SBIR Data Rights Period: May 31, 2026  *The Government’s rights to use, modify, reproduce, release, perform, display, or disclose technical data or computer software marked with this legend are restricted during the period shown as provided in paragraph (b)(4) of the Rights in Noncommercial Technical Data and Computer Software—Small Business Innovation Research (SBIR) Program clause contained in the above identified contract. No restrictions apply after the expiration date shown above. Any reproduction of technical data, computer software, or portions thereof marked with this legend must also reproduce the markings.*  **Distribution D:** Distribution authorized to Department of Defense and U.S. DoD Contractors only. Reason: To protect technical/operational data or information. SBIR Data Rights, 02/01/2019. Other requests shall be referred to RDER-NVG-MS.  **Export Control Warning:** This document contains technical data whose export is restricted by the Arms Export Control Act (Title 22, U.S.C., Sec 2751, et seq.) or the Export Administration Act of 1979, as amended (Title 50, U.S.C., App, 2401 et seq.) Violations of these export laws are subject to severe criminal penalties. Disseminate in accordance with provisions of DoD Directive 5230.25.  **Destruction Notice:** Destroy by any method that will prevent disclosure of contents or reconstruction of the document. |

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# 1.0 Introduction

To address the Army’s need for a squad-level system to detect and counter unmanned aerial systems (UASs), Intellisense Systems, Inc. (ISI) is developing a new Portable Anti-UAS (PAN‑UAS) device that combines state-of-the-art airspace monitoring technology with novel UAS countermeasure approaches and packages them in a man-packable system. Innovations in power reduction, miniaturization, and ruggedization of radar detection and radio frequency (RF) jamming systems will enable the PAN-UAS device to detect and counter both individual and swarms of UASs while being self-contained in a very portable form factor to directly address Army requirements. In this Phase II effort, ISI will develop the PAN-UAS system prototype, including its electronic circuits, embedded software, and mechanical enclosure, evaluate its performance, and demonstrate its operation. In the Phase I Transition period (February 1, 2019 to May 31, 2019), ISI defined the PAN-UAS system architecture, developed the MATLAB®/Simulink simulation model, and began development of the antenna and RF Module.

# 2.0 Technical Progress

## 2.1 Progress against Planned Milestones

The project is proceeding in accordance with the schedule shown in Figure 2-1. During this reporting period we began the Phase II project following the successful completion of the Transition (Phase I Option) phase and continued working on Tasks 2-5. Task 1 was completed and Milestone 1 was met during the Transition period.

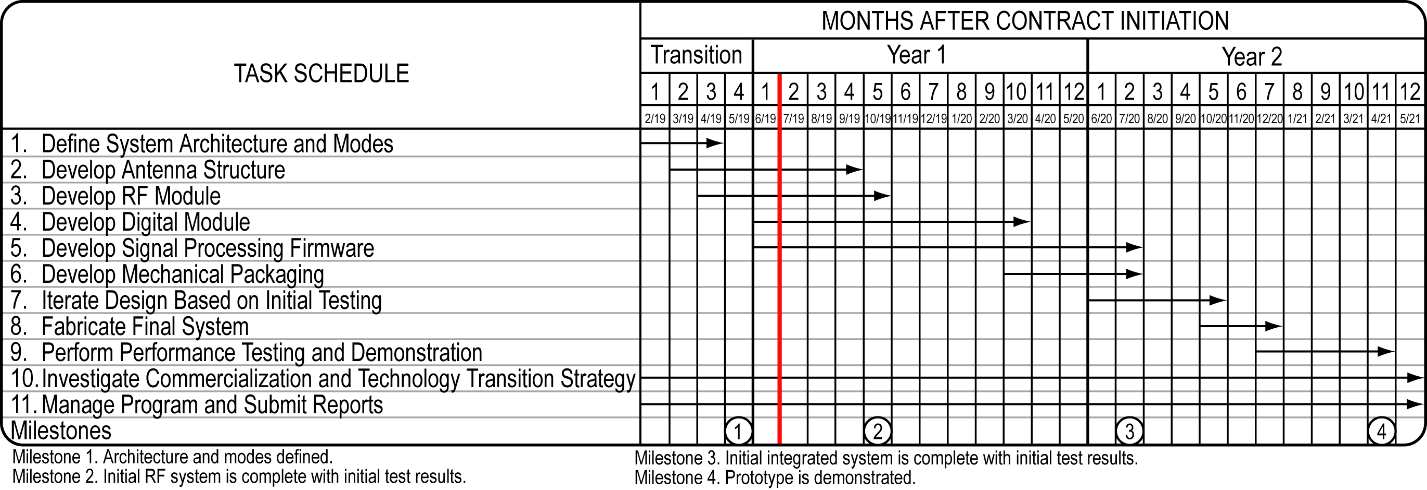


Figure 2-1. Performance schedule.

## 2.2 Results

During this period, ISI continued developing the PAN-UAS antenna, RF Module, and DSP algorithm. We concentrated on the following activities:

• Design and simulation of the radar antenna element (Task 2).

• Refinement of the RF Module design (Task 3).

• Refinement of the radar’s digital signal processing (DSP) algorithm, development of a Simulink simulation model (Task 4) and mapping of the model into a Zynq® Multi-Processor System-on-Chip (MPSoC) (Task 5).

• Planning of the initial prototype design and test (Task 3).

We started development of the initial prototype of the PAN-UAS radar by defining independent modules to enable block-level validation and incremental integration of the prototype. Our focus is on RF modules and antenna that will be built and tested before integration. Their development will be coordinated to enable connectivity and assembly of these boards. Figure 2-2 presents a top-level block diagram of the initial prototype of the PAN-UAS radar that will incorporate the following modules:

* 1. Antenna
  2. Transceiver (Transmitter – Receiver)
  3. Baseband/Digitizer
  4. Chirp RF Source
  5. Power (DC-DC Converters)
  6. DSP – ZCU106 Evaluation Kit
  7. Laptop-based software

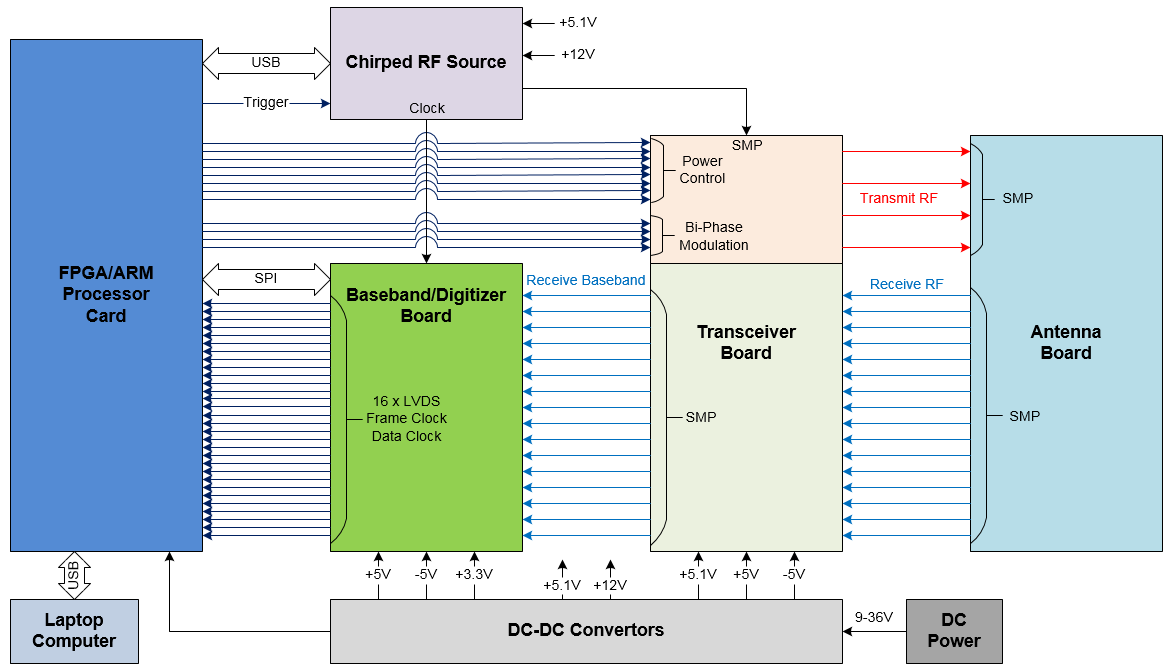


Figure 2-2. PAN-UAS initial prototype top-level block diagram.

### 2.2.1 Antenna Design (Task 2)

ISI worked with our consultant, Dr. Avakian, on design of the radar antenna element (Task 2). The modeling and simulation were done in HFSS. The initial design is shown in Figure 2-3. The optimal shape of the single element patch antenna is an octagon. We will use the low cost Rogers RO3730™ laminate material for the antenna printed circuit board (PCB) with  = 3 and tan = 0.0013, which are superior to the conventional FR4 material with  = 4.4 and tan = 0.02 and result in >2 dB extra gain. The resultant size of the antenna patch is 0.3λ – smaller than the original estimate.

|  |  |
| --- | --- |
| cid:image001.png@01D5343E.7FCC2680 | **Antenna Element Parameters**  • The substrate is 0.06 in. (1.52 mm) thick with  = 3  • The octagonal patch dimensions are  0.615×0.615 in.2 or 15.62×15.62 mm2.  • The feed is 50 Ω coaxial.  • The polarization is linear. |

Figure 2-3. Initial design of PAN-UAS radar antenna element developed by ISI.

The diagram in Figure 2-4 depicts the return loss for the antenna element with the minimum at 5.8 GHz carrier frequency and bandwidth (BW) of 200 MHz measured at -10 dB level. The 200 MHz bandwidth of the antenna element enables the radar to achieve 75 cm range resolution. A further increase of the antenna bandwidth can be achieved by adding a buried layer that is connected to the feed and is coupled with the octagon patch on the top layer of the antenna PCB. Another way to increase the antenna is to add a notch of a rectangular or other shape. We will explore these approaches if the simulation results for the antenna array with the initial octagonal patch design are not satisfactory.

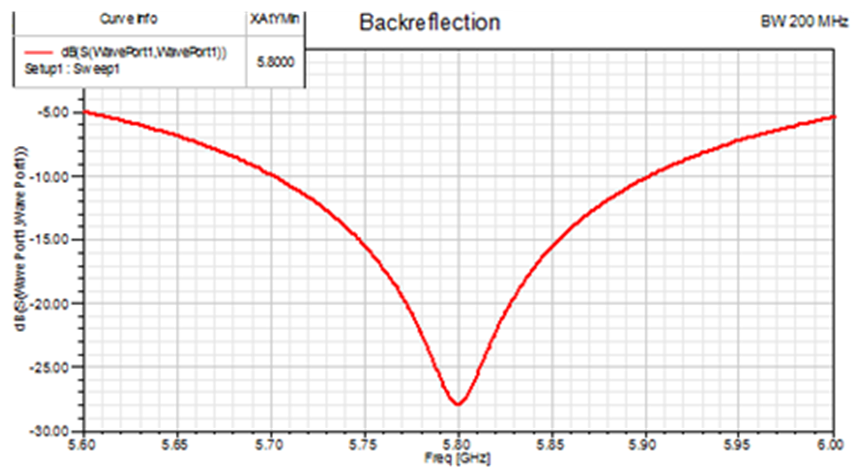
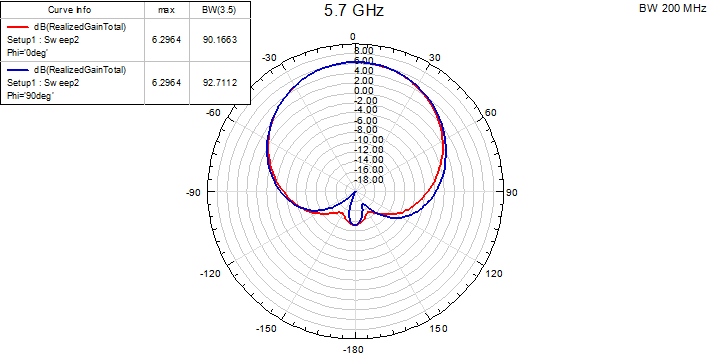
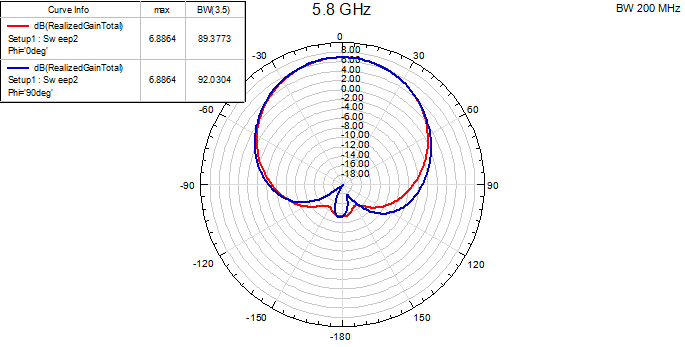


Figure 2-4. Radar antenna - RF transceiver plan.

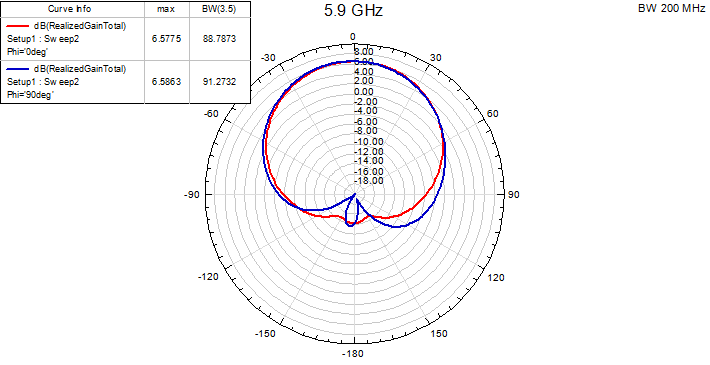
Beam diagrams in Figure 2-5 show the antenna beam pattern at 5.8 ± 0.1 GHz frequency for vertical and horizontal polarizations (red and blue curves, respectively, for the antenna element with the feed point shifted to the right from the center). The simulation results show 90 degrees beamwidth in both coordinates for 5.7-5.9 GHz band and the gain exceeding the planned 5 dB (6.89 dB at 5.8 GHz center frequency).



(a)



(b)



(c)

Figure 2-5. Antenna pattern simulation for (a) 5.7, (b) 5.8, and (c) 5.9 GHz frequencies and 200 MHz BW.

The next step in antenna design will be simulation of the TX and RX arrays and analysis of the interactions of antenna elements.

### 2.2.2 RF Module Design (Task 3)

Following the approach of incremental design and integration of the initial prototype illustrated in Figure 2-2, we divided the RF Module into four PCBs: Chirped RF Source, Transceiver, Baseband/Digitizer, and Antenna Array shown in Figure 2-6. We will develop, manufacture, and test each of these boards before integrating them into the initial prototype. We expect that some of these boards will have two (or more) revisions.

During this reporting period we updated the RF Module design and identified all of the main components. Addressing the recommendation from the Phase I Option Final Report, we evaluated Texas Instruments’ recently introduced LMX2572, a 6.4 GHz phase locked loop (PLL) synthesizer with chirp capability that has an integrated voltage-controlled oscillator (VCO). However, this device requires frequent calibration and is not suitable for our applications.

We analyzed other components and improved the Chirp RF Source design by replacing the VCO circuit with the new MAOC 009259 device from MACOM. This change not only simplifies the circuit and improves its performance by reducing the phase noise, but also decreases the power consumption.

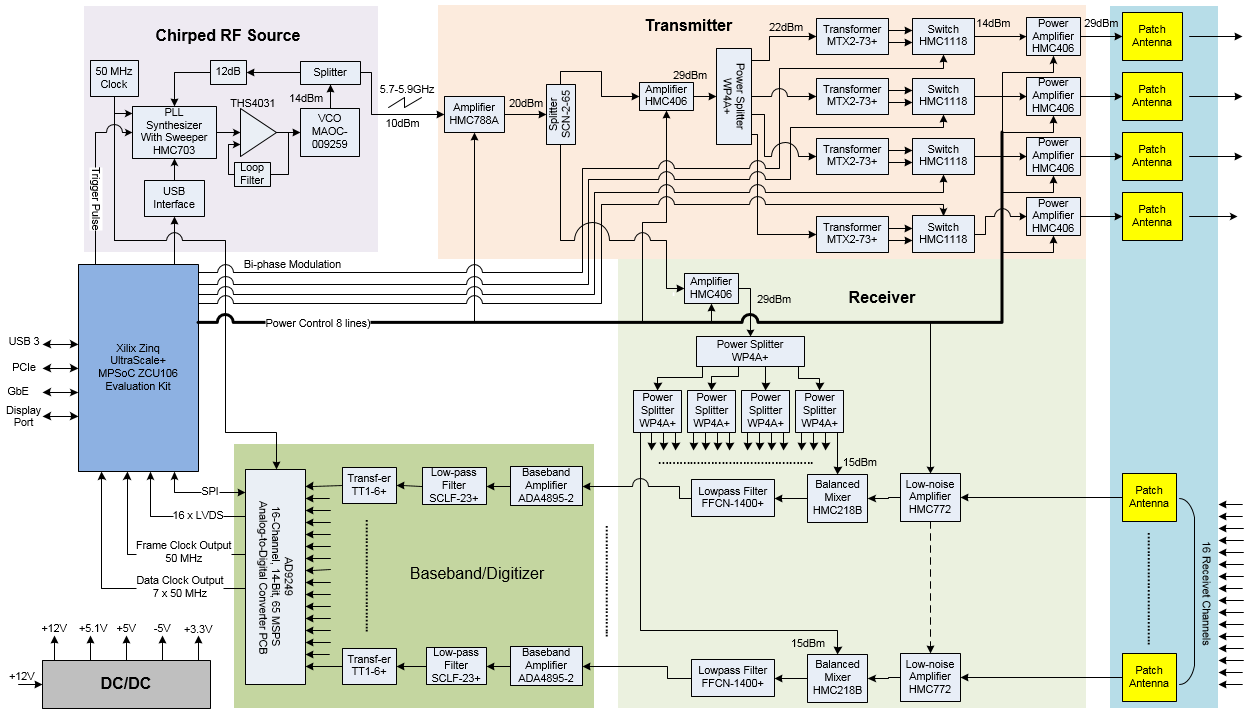


Figure 2-6. Detailed block diagram of the initial prototype. The updated RF Module design has of all the main components identified.

### 2.2.3 Algorithms (Tasks 4 and 5)

We updated the DSP algorithm for the PAN-UAS MIMO radar. Figure 2-7 depicts the flow diagram, which shows the algorithm partitioned into hardware accelerated implementation in Zynq® programmable logic and software functions executed by Zynq’s Arm® processor cores.

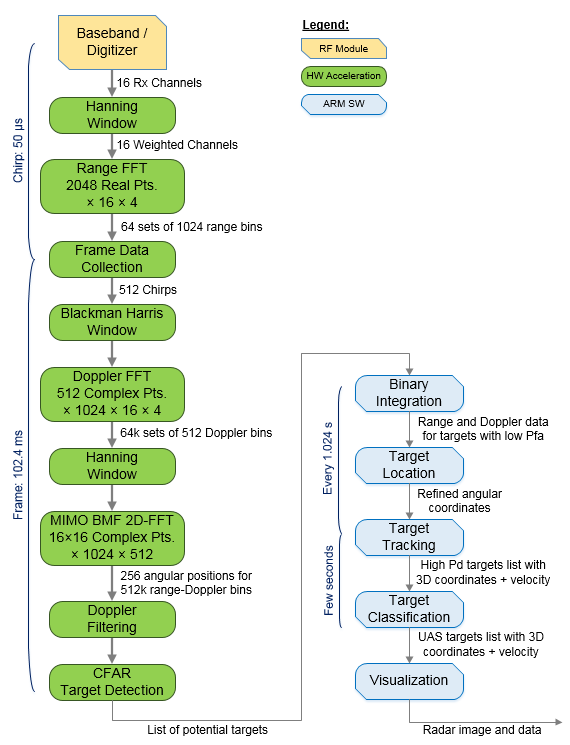


Figure 2-7. DSP Simulink model – current state.

In the first version of the radar design we will use a time separation of four transmitters for MIMO operation to simplify the algorithm design and system testing and reduce the power consumption. In this mode the chirp duration is 50 µs and a four-chirp cycle period is 200 µs. In the final version we will use a MIMO operation with phase code separation of the transmitters with a 100 µs chirp that will increase the detection range by 40% and double the maximum target velocity. The design modification required to switch between the transmitter separation methods will be limited to the algorithm (firmware and software) and will not require any hardware changes. The algorithm will be refined during the development and testing.

**DSP Algorithm in Simulink and Zynq®**

We continued refining the Simulink model and mapping it to the FPGA-based Zynq® MPSoC. The current model (Figure 2-8) has a two-dimensional (2D) Fast Fourier Transform (FFT) and supports range and Doppler calculations. Integration and testing of data acquisition capabilities using an analog-to-digital converter (ADC) evaluation board (AD9681) and a Zynq**®** evaluation board ZC706 is in progress. To accommodate the large amount of data, we use external DDR3 memory as a data buffer.

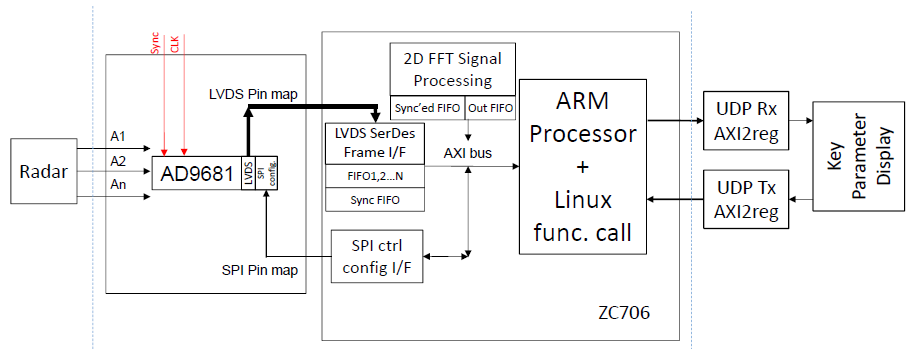


Figure 2-8. DSP Simulink model – current state.

### 2.2.4 Test Plan (Task 3)

We have prepared a plan for testing the RF Module blocks (see Tables 2-1, 2-2, 2-3, and 2-4) before their integration in the prototype. The diagrams in Figures 2-9, 2-10, 2-11, and 2-12 illustrate the test setup for each module under test. As Chirp RF Source module is used in all test setups, we will evaluate its performance and validate its functionality by comparing it with the evaluation board results. This approach also decouples the test of other modules from the maturity of Chirp RF Source PCB circuit.

Completion of these tests will constitute Milestone 2 (planned for October 2019) and enable integration of the RF Module with the Digital Module and DSP algorithm. The test plan for the initial prototype will be defined later and executed to complete the design validation and evaluation and achieve Milestone 3 planned for July 2020.

Table 2-1. Radar Antenna Test Plan

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Required** | **Time** | **Test Equipment** | **Test Condition** |
| Return Loss, dB | -10 (T) /  -15 (O) | 08/19 | Network analyzer or its equivalent. | Lab test. Frequency BW: 5800+/‑100 MHz (T),  5800+/‑150 MHz (O). |
| Transmit/Receive Isolation, dB | ≥40 | 08/19 | Network analyzer or its equivalent. | Lab test. Frequency bandwidth: 5800+/-150 MHz |
| Single element gain, dB | ≥5 | 09/19 | 12-in. trihedral corner reflector. Chirped RF source. Balanced mixer. Oscilloscope. | Outside test with corner reflector in two-way mode and FMCW modulation/demodulation. Gain is calculated by using the transmit/receive signal ratio, the reflector’s RCS, and the range value. |
| Single element bandwidth, MHz | ±100 (T) /  ±150 (O) | 09/19 | 12-in. trihedral corner reflector. Chirped RF source. Balanced mixer. Oscilloscope. | Outside test with corner reflector in two-way mode and FMCW modulation/demodulation. Modulation bandwidth is increased until 2 dB signal decrease. Measurement will be done with normal and ±45° positions. |
| Single element beam-width, degree | ≥90 | 09/19 | 12-in. trihedral corner reflector. Turn-table with angular scale. Chirped RF source. Balanced mixer. Oscilloscope. | Outside test with corner reflector in two-way mode and FMCW modulation/demodulation. Turntable with antenna will be applied to obtain beam pattern. -6 dB two-way beam-width will be determined. |
| Four element gain, dB | ≥11 | 09/19 | The same as for single element gain test, plus 4-way power combiner. | The same setup as for single element gain test, but with signals from four antennas being combined. |
| Four element bandwidth, MHz | ±100 (T) / ±150 (O) | 09/19 | The same as for single element bandwidth test, plus 4-way power combiner. | The same setup as for single element bandwidth test, but with signals from four antennas being combined. |
| Four element beam-width, degree | ≤30 | 09/19 | The same as for single element beam-width test, plus 4-way power combiner. | The same setup as for single element beam-width test, but with signals from four antennas being combined. |
| 2×4 MIMO  beam-width, degree | ≤15 | 09/19 | The same as for four element beam-width test. | The same way as for four element beam-width test, but with two transmit positions recorded and summarized. |

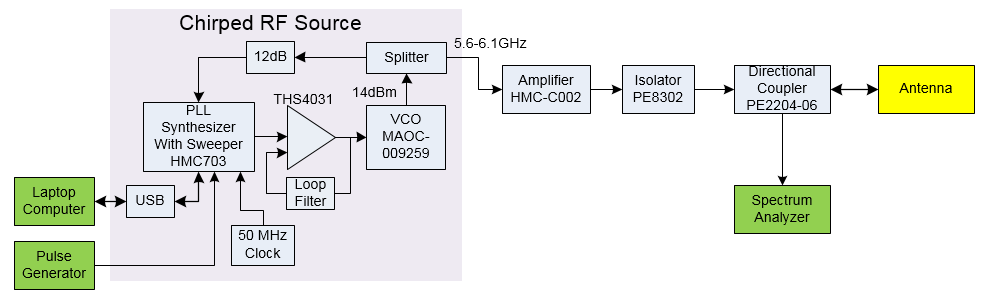


Figure 2-9. Antenna return loss test setup.

Table 2-2. Radar Chirped RF Source Test Plan

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Required** | **Time** | **Test Equipment** | **Test Condition** |
| Phase noise at 10 MHz offset, dBc/Hz | ≤-135 | 09/19 | Spectrum analyzer | Frequency multiplier and downconverter may be applied to overcome spectrum analyzer limit. |
| Phase noise at 10 kHz offset, dBc/Hz | ≤-100 | 09/19 | Spectrum analyzer |
| Maximum modulation bandwidth, MHz | ≥300 | 09/19 | Spectrum analyzer, pulse generator | 5800 MHz central frequency, 100 μs modulation period. |
| Minimum modulation period, μs | ≤-50 | 09/19 | Spectrum analyzer, pulse generator | 5800 MHz central frequency, 300 MHz modulation bandwidth. |
| Chirp return time, μs | ≤-10 | 09/19 | Oscilloscope, pulse generator | Measure the chirp transient time with Vtune signal of the VCO during the chirp modulation. 5800 MHz central frequency, 300 MHz modulation BW, 100 μs modulation period. |
| Power consumption, W | ≤1.2 | 09/19 | Power supply unit with current indicator | 5800 MHz central frequency, 300 MHz modulation bandwidth. |

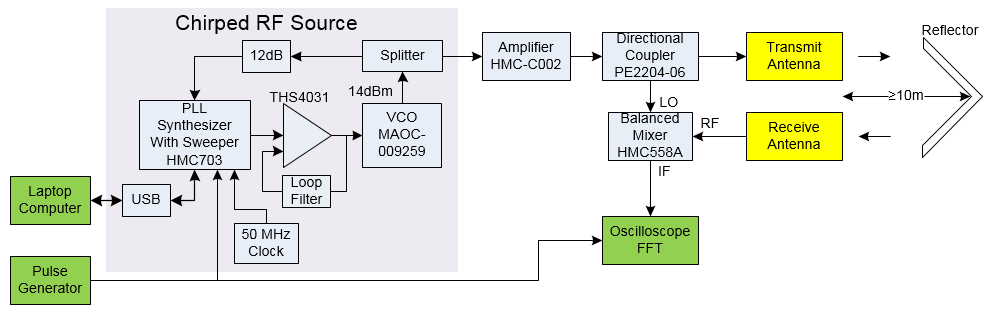


Figure 2-10. Antenna gain/bandwidth/beamwidth test setup.

Table 2-3. Radar Transmitter Test Plan

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Required** | **Time** | **Test Equipment** | **Test Condition** |
| Output power, dBm | ≥28 | 10/19 | Chirped RF source, spectrum analyzer | 5800 MHz central frequency, 300 MHz modulation bandwidth, 5 dBm input power. All four channel outputs will be measured. |
| Bi-phase modulation amplitude/phase unbalance | ≤1 dB,  ≤10° | 10/19 | Chirped RF source, I/Q mixer, oscilloscope | Amplitude/phase unbalance in all four channel outputs will be measured |
| Output power in power-down mode, dBm | ≤0 | 10/19 | Chirped RF source, spectrum analyzer | All four channel outputs will be measured with 5 dBm input power level. |
| Power consumption with four channel outputs, W | ≤12 | 10/19 | Power supply unit with current indicator | 5800 MHz central frequency, 300 MHz modulation bandwidth, 5 dBm input power. 50 Ω loads on all outputs. |
| Power consumption with single channel output, W | ≤5 | 10/19 | Power supply unit with current indicator | 5800 MHz central frequency, 300 MHz modulation bandwidth, 5 dBm input power. 50 Ω loads on all outputs. |
| Power consumption in power down mode, W | ≤0.3 | 10/19 | Power supply unit with current indicator | 5800 MHz central frequency, 300 MHz modulation bandwidth, 5 dBm input power. Power down for all amplifiers. |

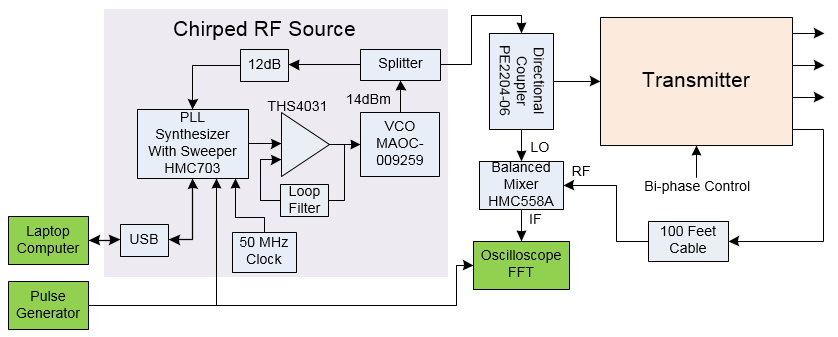


Figure 2-11. Transmitter bi-phase modulation amplitude/phase unbalance test setup.

Table 2-4. Radar Receiver Test Plan

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Required** | **Time** | **Test Equipment** | **Test Condition** |
| Double sideband noise figure, dB | ≤3 | 10/19 | Chirped RF source, calibrated noise source, baseband amplifier, oscilloscope | 5800 MHz central frequency, 300 MHz modulation bandwidth, 14 dBm input LO power. 50 Ω loads on inputs if noise source is not connected. All 16 channels will be measured. |
| Total receiver gain, dB | 40±2 | 10/19 | Chirped RF source, baseband amplifier, oscilloscope, spectrum analyzer, 100 ft coax cable, RF attenuator | 5800 MHz central frequency, 300 MHz modulation bandwidth, 14 dBm input LO power. Part of the LO signal connected to the receiver input through 100 ft cable. Input/output power is measured with spectrum analyzer/oscilloscope. All 16 channels will be measured. |
| Input P1dB, dBm | ≥-32 | 10/19 | Chirped RF source, baseband amplifier, oscilloscope, spectrum analyzer, 100 ft coax cable, RF attenuator kit | 5800 MHz central frequency, 300 MHz modulation bandwidth, 14 dBm input LO power. Part of the LO signal connected to the receiver input through 100 ft cable. Input/output power is measured with spectrum analyzer/oscilloscope. All 16 channels will be measured. |
| Power consumption in full operation mode, W | ≤6 | 10/19 | Power supply unit with current indicator | 5800 MHz central frequency, 300 MHz modulation bandwidth, 14 dBm input LO power. |
| Power consumption in power down mode, W | ≤0.1 | 10/19 | Power supply unit with current indicator | 5800 MHz central frequency, 300 MHz modulation bandwidth, 14 dBm input LO power. Power down for all amplifiers. |

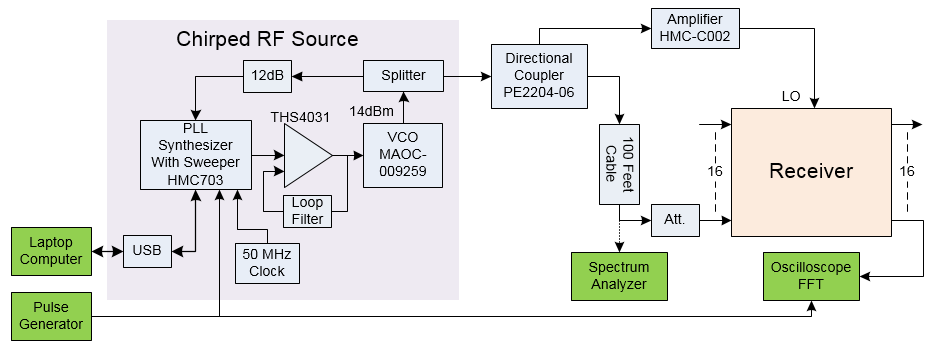


Figure 2-12. Receiver gain/P1dB/unbalance test setup.

## 2.3 Problem Areas Affecting Technical Elements

No problem areas affecting technical elements were identified. ISI is tracking the risks including deviations from the size, weight, and power (SWaP) specifications.

## 2.4 Problem Areas Affecting Cost Elements

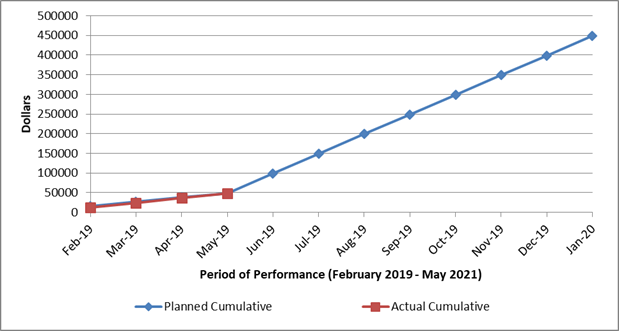
No problem areas affecting cost elements were identified.

## 2.5 Trips

No trips were taken during this reporting period.

# 3.0 FINANCIAL INFORMATION

Of the total funded transition amount of $48,922.00, the amount to be invoiced for this reporting period is $12,322.00. The cumulative invoiced amount will be $48,922.00. The CPFF SBIR Phase II effort began 06/01/19. Our Finance Department is currently completing the month-end closeout for June. We will include the financial information for June in the next report. The number of labor hours expended through 05/31/19 is 12.50. The total number of labor hours expended through 05/31/19 is 223.55.



# 4.0 Plans for Activities During the Following Reporting Period

In the next reporting period, ISI will continue working on development of antenna (Task 2) by scaling the model to 2x2 TX and 4x4 RX arrays. We will also continue development of RF Module (Task 3) and begin schematic design of the RF PCBs. We plan to complete the single channel DSP Simulink model (Task 5) and continue the effort to map it into Zynq MPSoC (Task 4).

# 5.0 NAME AND TELEPHONE NUMBER OF PREPARER OF THE REPORT

Preparer: Alexander Genusov

Telephone Number: (310) 320-1827, ext. 272